

In re Patent Application of:
POMET ET AL.
Serial No. 09/727,300
Filing Date: NOVEMBER 30, 2000

REMARKS

The Examiner is thanked for the thorough examination of the present application. Each of the independent claims has been amended to more clearly define over the prior art. No new matter is added and no new issues are believed raised by the amendments.

The patentability of the claims is discussed in greater detail below. Favorable reconsideration is respectfully requested.

I. The Claimed Invention

Amended independent Claim 12, for example, is directed to an electronic device comprising a central processing unit, a one peripheral device, and a data bus connected between the peripheral device and the central processing unit through which data travels at a rate of a clock signal. The electronic device also comprises a transmission line connected between the peripheral device and the central processing unit in parallel with said data bus and for providing a random signal thereto that is synchronous with the clock signal. The central processing unit and the peripheral device each comprises a data encryption/decryption cell connected to the data bus and to the transmission line for generating a same current secret key at each clock cycle based upon the random signal.

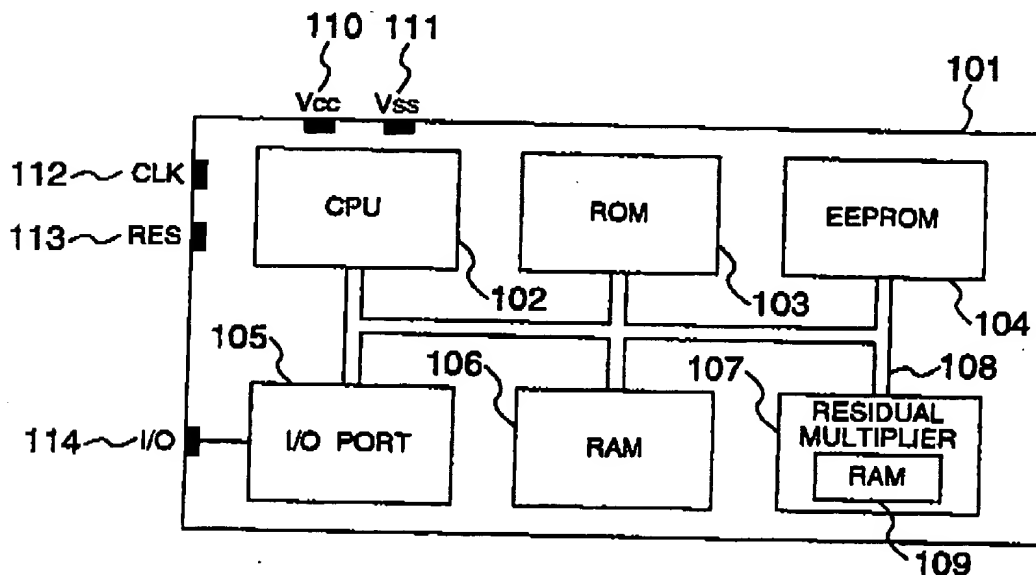
Amended independent Claim 25 is similar to Claim 12 except the peripheral device comprises a memory device. Amended independent Claim 34 is also similar to Claim 12 and

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is directed to a smart card. Amended independent 42 is a method counterpart to Claim 12.

II. The Claims Are Patentable

The Examiner rejected all of the independent claims as unpatentable over the Miyazaki et al. patent. The Examiner correctly notes the Miyazaki et al. patent discloses a central processing unit 102, a peripheral device (not specifically indicated), a data bus 108, and a transmission line connected at I/O 114 as is shown below in FIG. 1 from the patent.



In contrast, amended independent Claim 12, for example, is directed to a data bus connected between the peripheral device and the central processing unit through which data travels at a rate of a clock signal, and a transmission line connected between the peripheral device and

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the central processing unit in parallel with the data bus and for providing a random signal thereto that is synchronous with the clock signal. In other words, the data bus and the transmission line are in parallel with each other between the CPU and the peripheral device.

The Miyazaki et al. patent fails to disclose the data bus and the transmission line in parallel between the CPU and the peripheral device. Instead, the Miyazaki et al. patent discloses the data bus in series with the transmission line between the CPU and the peripheral device.

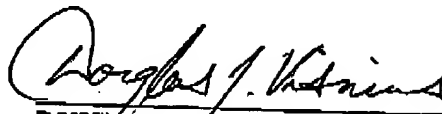
Independent Claims 25, 34, and 42 include recitations similar to Claim 12. Accordingly, amended independent Claims 12, 25, 34, and 42 are patentable. The dependent claims, which recite yet further distinguishing features of the invention, are also patentable, and require no further discussion.

CONCLUSIONS

In view of the amendments to the claims and the arguments presented above, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned at the telephone number listed below.

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Respectfully submitted,



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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has
been forwarded via facsimile number 571-273-8300 to the
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-
1450 this 21st day of October, 2005.

